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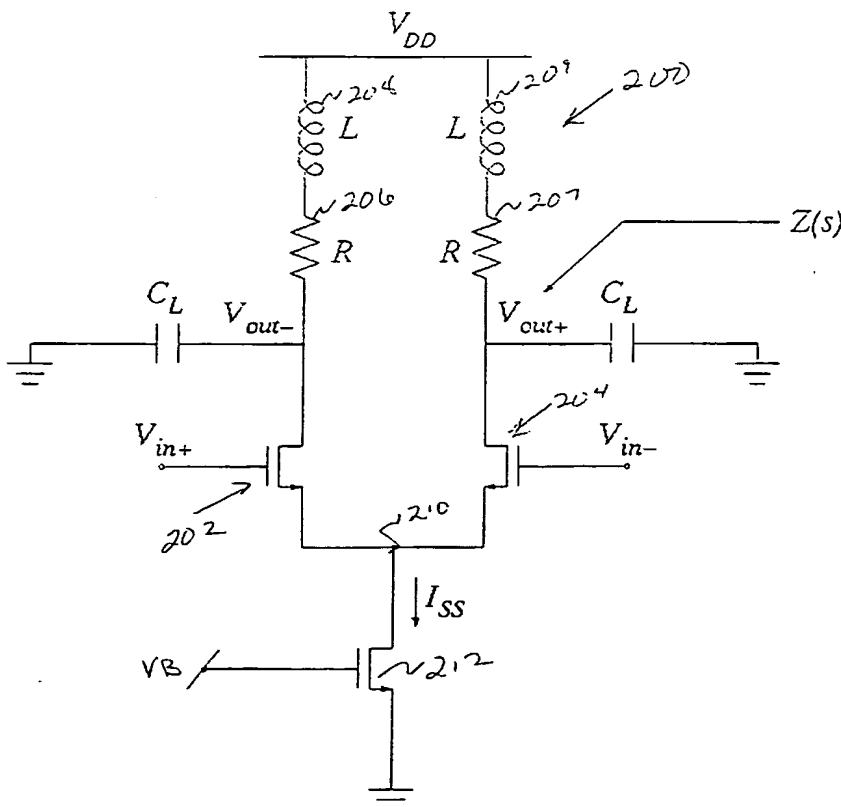
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(54) Title: CURRENT-CONTROLLED CMOS CIRCUITS WITH INDUCTIVE BROADBANDING



(57) Abstract: Various circuit techniques for implementing ultra high speed circuits use current-controlled CMOS (C<sup>3</sup>MOS) logic with inductive broadbanding fabricated in conventional CMOS process technology. Optimum balance between power consumption and speed for each circuit application is achieved by combining high speed C<sup>3</sup>MOS logic with inductive broadbanding /C<sup>3</sup>MOS logic with low power conventional CMOS logic. The combined C<sup>3</sup>MOS logic with inductive broadbanding /C<sup>3</sup>MOS /CMOS logic allows greater integration of circuits such as high speed transceivers used in fiber optic communication systems.

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## CURRENT-CONTROLLED CMOS CIRCUITS WITH INDUCTIVE BROADBANDING

### 5 CROSS-REFERENCES TO RELATED APPLICATIONS

This application is a continuation of and claims the benefit of U.S. provisional patent application No. 60/184,703, filed February 24, 2000, the disclosure of which is incorporated herein by reference.

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### BACKGROUND OF THE INVENTION

The present invention relates in general to high speed logic circuitry, and in particular to current-controlled CMOS (or C<sup>3</sup>MOS™) logic circuits with inductive broadbanding.

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For a number of reasons CMOS is the logic family of choice in today's VLSI devices. Due to the complementary nature of its operation, CMOS logic consumes zero static power. CMOS also readily scales with technology. These two features are highly desirable given the drastic growth in demand for low power and portable electronic devices. Further, with the computer aided design (CAD) industry's focus on developing automated design tools for CMOS based technologies, the cost and the development time of CMOS VLSI devices has reduced significantly.

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The one drawback of the CMOS logic family, however, remains its limited speed. That is, conventional CMOS logic has not achieved the highest attainable switching speeds made possible by modern sub-micron CMOS technologies. As a result of the speed limitations of conventional CMOS logic, integrated circuit applications in the Giga Hertz frequency range have had to look to alternative technologies such as ultra high speed bipolar circuits and Gallium Arsenide (GaAs). These alternative technologies, however, have drawbacks of

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their own that have made them more of a specialized field with limited applications as compared to silicon MOSFET that has had widespread use and support by the industry. In particular, compound semiconductors such as GaAs are more susceptible to defects that degrade device performance, and suffer from increased gate leakage current and reduced noise margins. Furthermore, attempts to reliably fabricate a high quality oxide layer using GaAs have not thus far met with success. This has made it difficult to fabricate GaAs FETs, limiting the GaAs technology to junction field-effect transistors (JFETs) or Schottky barrier metal semiconductor field-effect transistors (MESFETs). A major drawback of the bipolar technology, among others, is its higher current dissipation even for circuits that operate at lower frequencies.

### SUMMARY OF THE INVENTION

A significant improvement in speed of operation of CMOS circuitry has been achieved by a family of CMOS logic that is based on current-controlled mechanism. Current-controlled CMOS (or C<sup>3</sup>MOS) logic is described in greater detail in commonly-assigned patent application number 09/484,856 (Atty Dkt No. 019717-000310), entitled "Current-Controlled CMOS Logic Family," by Hairapetian, which is hereby incorporated in its entirety for all purposes. The basic building block of the C<sup>3</sup>MOS logic family uses a pair of conventional MOSFETs that steer current between a pair of load devices in response to a difference between a pair of input signals. Thus, unlike conventional CMOS logic, C<sup>3</sup>MOS logic dissipates static current, but operates at much higher speeds.

According to one aspect of the invention, to further enhance speed of operation of circuits implemented in CMOS technology, the present invention introduces inductive elements in the C<sup>3</sup>MOS circuits. In a specific embodiment, a spiral inductor is inserted in series with the load devices of selected C<sup>3</sup>MOS structures that process high-bandwidth data signals. The resulting series combination of inductor and resistive element (e.g., polysilicon resistors) that is in

parallel with an existing capacitive load provides a high impedance at a higher bandwidth than would be possible without the presence of the inductor. Optimized values for the inductors ensure appropriate placement of the circuit's natural frequencies in the complex plane to achieve fast rise and fall times with appropriate overshoot and undershoot. The present invention combines the use of this type of shunt peaking with C<sup>3</sup>MOS circuits that process broadband bi-level (i.e., digital as opposed to analog) differential signals. The combination of these characteristics allows for improvement of the output signal's inter-symbol interference without any increase in power dissipation.

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According to another aspect of the invention, a multiplexer circuit includes C<sup>3</sup>MOS with inductive broadbanding to facilitate operation at ultra-high frequencies.

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According to another aspect of the invention, a flip-flop is implemented utilizing C<sup>3</sup>MOS with inductive broadbanding to operate at ultra-high frequencies.

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According to another aspect of the invention, a complementary metal-oxide-semiconductor (CMOS) logic circuitry combines on the same silicon substrate, current-controlled MOSFET circuitry of the type described above for high speed signal processing, with conventional CMOS logic that does not dissipate static current. Examples of such combined circuitry include serializer/deserializer circuitry used in high speed serial links, high speed phase-locked loop dividers, and the like.

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Other features and advantages of the invention will be apparent in view of the following detailed description and appended drawings.

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## BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic diagram of differential pair including inductive broadbanding implemented with CMOS technology;

5 Fig. 2(a) is a schematic diagram of the circuit of Fig. 1 without the shunt inductor;

Fig. 2(b) is a simplified diagram depicting the transient behavior of the circuit of Fig. 2(a);

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Fig. 2(c) is a graph depicting the difference between ideal and C<sup>3</sup>MOS step responses;

Fig. 3 is a graph depicting the step response of the circuit of Fig. 1  
15 for four values of series inductance;

Fig. 4(a) is a graph depicting inter-symbol interference (ISI) vs. input pulse width for five values of series inductance;

20 Fig. 4(b) is a graph depicting the output signal of the circuit of Fig. 1 with and without inductors;

Fig. 5 is shows a block diagram for a circuit that combines C<sup>3</sup>MOS with inductive broadbanding, C<sup>3</sup>MOS, and conventional CMOS logic on a single  
25 silicon substrate to achieve optimum tradeoff between speed and power consumption;

Fig. 6(a) is a schematic diagram of a serializer circuit utilizing features of the invention;

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Fig. 6(b) is a more detailed depiction of the 2:1 MUX depicted in Fig. 6(a);

Fig. 7 is a circuit diagram of a MUX utilizing features of the present invention;

Fig. 8 is a circuit diagram of a flip-flop utilizing features of the invention; and

Fig. 9 is a simplified block diagram of a transceiver system that utilizes the C<sup>3</sup>MOS with inductive broadbanding/C<sup>3</sup>MOS/CMOS combined logic according to the present invention to facilitate interconnecting high speed fiber optic communication channels.

## DESCRIPTION OF THE SPECIFIC EMBODIMENTS

The present invention provides ultra high-speed logic circuitry implemented in silicon complementary metal-oxide-semiconductor (CMOS) process technology. A distinction is made herein between the terminology “CMOS process technology” and “CMOS logic.” CMOS process technology as used herein refers generally to a variety of well established CMOS fabrication processes that form a field-effect transistor over a silicon substrate with a gate terminal typically made of polysilicon material disposed on top of an insulating material such as silicon dioxide. CMOS logic, on the other hand, refers to the use of complementary CMOS transistors (n-channel and p-channel) to form various logic gates and more complex logic circuitry, wherein zero static current is dissipated. The present invention uses current-controlled mechanisms with inductive broadbanding to develop a family of very fast current-controlled CMOS (or C<sup>3</sup>MOS™) with inductive broadbanding logic that can be fabricated using a variety of conventional CMOS process technologies, but that unlike conventional CMOS logic does not dissipate static current. C<sup>3</sup>MOS with inductive broadbanding

logic or current-controlled metal-oxide-semiconductor field-effect transistor (MOSFET) logic are used herein interchangeably.

In a preferred embodiment, the basic building block of this logic family is an NMOS differential pair with series connected inductive/resistive (LR) loads.

Figure 1 illustrates the basic C<sup>3</sup>MOS differential pair 200 with shunt inductors  $L$ , and load capacitors  $C_L$ . A pair of n-channel MOSFETs 202 and 204 receive differential logic signals  $V_{in+}$  and  $V_{in-}$  at their gate terminals, respectively. Resistive loads 206 and 207 in series with shunt inductors 208 and 209 connect the drain terminals of MOSFETs 202 and 204, respectively, to the power supply VDD. Drain terminals of MOSFETs 202 and 204 form the outputs  $V_{out-}$  and  $V_{out+}$  of the differential pair, respectively. In a preferred embodiment, the shunt inductors 208 and 209 are spiral inductors coupled to the substrate utilizing standard techniques. Resistive loads 206 and 207 may be made up of either p-channel MOSFETs operating in their linear region, or resistors made up of, for example, polysilicon material. In a preferred embodiment, polysilicon resistors are used to implement resistive loads 206 and 207, which maximizes the speed of differential pair 200. The source terminals of n-channel MOSFETs 202 and 204 connect together at node 210. A current-source n-channel MOSFET 212 connects node 210 to ground (or negative power supply). A bias voltage  $V_B$  drives the gate terminal of current-source MOSFET 212 and sets up the amount of current  $I$  that flows through differential pair 200. In response to the differential signal at  $V_{in+}$  and  $V_{in-}$ , one of the two input n-channel MOSFETs 202 and 204 switches on while the other switches off. All of current  $I$ , thus flows in one leg of the differential pair pulling the drain terminal ( $V_{out+}$  or  $V_{out-}$ ) of the on transistor down to logic low, while the drain of the other (off) transistor is pulled up toward logic high. Shunt peaking, according to the present invention, can be selectively applied to those parts of an integrated circuit that require the bandwidth enhancement.



In Fig. 1, the input levels  $V_{in+}$  and  $V_{in-}$  vary symmetrically in opposite directions when a digital signal is received. For example if  $V_{in+}$  swung positive then  $V_{in-}$  would swing negative. The voltage levels at  $V_{out-}$  and  $V_{out+}$  swing in the same direction as the respective input signal levels. For reasons  
5 described more fully below, for broadband signals including frequencies in the range of over 5 GigaHz the transient response of the circuit must be fast.

Figs. 2(a) and (b) respectively depict the circuit of Fig. 1 with the inductors removed, resulting in a  $C^3$ MOS buffer, and a simple equivalent circuit  
10 illustrating the transient behavior of the circuit. In this case the output transient waveform is characterized by an exponential waveform with a time constant  $RC$ . This waveform is depicted in Fig. 2(c) with a label " $C^3$ MOS" and has an initial slope of  $I/C_L$ . The difference between the ideal and exponential step response is also depicted in Fig. 2(c).

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In the circuit of Fig. 2(a) the transient response of the output signal would be controlled by the  $RC$  time constant. It is clear from Fig. 2(c) that the presence of the load resistor significantly slows down the transient step response. Thus, when an input signal is received with a very fast rise time the current  
20 increases rapidly to charge or discharge the load capacitor. However, the transient response of the output signal is controlled by the  $RC$  time constant and can have a longer rise time than the input pulse.

Now, considering the circuit as disclosed in Fig. 1, including the  
25 inductors, as is well-known in the art an inductor resists a change in current. Thus, when the drain current changes in response to an input signal the inductor chokes off current flow through the resistor so that the capacitor discharges rapidly to generate an output signal with a small rise time.

The larger the value of series inductance, the longer the full value of the current is available to charge/discharge the load capacitances. Fig. 3 shows the step response for 4 different values of series inductance.

5 From Fig. 3 it is clear that higher values of inductance decrease the rise time. However, if the inductance value becomes too large, an excessive overshoot will occur. To determine the optimum value of inductance, the pulse response for a set of input pulses is observed with varying pulse widths. The graphs in Fig. 4(a) show the relative error between output and input pulse widths  
10 (referred to as intersymbol interference or ISI) for 4 values of inductance.

From the Fig. 4(a) graphs it is apparent that given the values of R and C<sub>L</sub>, the optimum inductor value is given by:

15 
$$L_{S(opt)} = (0.35) * C_L R^2$$

Fig. 4(b) depicts the output signals for the circuit of Fig. 1 with and without the inductors. The magnitude of the time intervals between zero crossing points of the output signal provide important information for interpreting the input  
20 signal. As depicted in Fig. 4(b), the slope of the waveform zero-crossings is sharper when the inductors are included in the circuit thereby more precisely defining the time intervals between zero-crossing points and reducing inter-symbol interference.

25 In one embodiment of the present invention a transceiver circuit along a fiber optic channel deserializes an input data stream with a bit rate of, for example, 10 Gb/s. After processing the lower frequency deserialized data, the data is serialized before transmission back onto the fiber channel. According to the present invention, those parts of this circuitry that process the highest speed data  
30 (e.g., input to the deserializer and output of the serializer) are implemented by C<sup>3</sup>MOS circuitry with inductive broadbanding.

Figure 5 shows a simplified block diagram illustrating this exemplary embodiment of the invention. A C<sup>3</sup>MOS with inductive broadbanding input circuit 40 receives a high frequency input signal IN and outputs a first divided down version of the signal IN/n. A C<sup>3</sup>MOS MUX 42 then receives this first divided down version and divides the received signal down by another factor of m to output a second divided down version of the signal IN/(n x m). The lower frequency signal IN/(n x m) is then processed by core circuitry 44 that is implemented in conventional CMOS logic. The low frequency signal from the core logic is then increased in frequency by the reverse process to form an output signal at the original high input frequency.

Figure 6(a) shows an exemplary 16:1 serializer according to the present invention. The serializer includes a 16:8 multiplexer 50 that converts the data rate to 1.25 Gb/s, followed by an 8:4 multiplexer 54 that converts the data rate to 2.5Gb/s. The 2.5Gb/s data is further converted to a 5Gb/s data by a 4:2 multiplexer 56, and finally to a 10Gb/s data by a 2:1 multiplexer 58. A flip flop 60 at the output re-times the 10Gb/s data to generate the final output data stream.

According to this embodiment of the invention, the circuit of Figure 6(a) may combine conventional CMOS logic used for the lower speed multiplexers and core processing circuitry, with C<sup>3</sup>MOS logic for the mid-rate multiplexers, and C<sup>3</sup>MOS logic with inductive broadbanding for the highest speed multiplexer (i.e., the 2:1 multiplexer 58) as well as the output re-timing flip flop 60.

As illustrated by the various C<sup>3</sup>MOS with inductive broadbanding logic elements described below, all of the building blocks of any logic circuitry can be constructed using the C<sup>3</sup>MOS with inductive broadbanding technique of the present invention. More complex logic circuits such as shift registers, counters, frequency dividers, etc., can be constructed in C<sup>3</sup>MOS with inductive broadbanding using the basic elements described above. As mentioned above,

however, both C<sup>3</sup>MOS and C<sup>3</sup>MOS with inductive broadbanding logic does consume static power. Additionally, the fabrication of C<sup>3</sup>MOS with inductive broadbanding logic is more expensive than C<sup>3</sup>MOS or CMOS because of the need to add inductors to the IC.

5

The static current dissipation of C<sup>3</sup>MOS and/or C<sup>3</sup>MOS with inductive broadbanding may become a limiting factor in certain large scale circuit applications. In one embodiment, as depicted for example in Figs. 5 and 6(a), the present invention combines C<sup>3</sup>MOS with inductive broadbanding and C<sup>3</sup>MOS logic with conventional CMOS logic to achieve an optimum balance between speed and power consumption. According to this embodiment of the present invention, an integrated circuit utilizes C<sup>3</sup>MOS with inductive broadbanding logic for the ultra high speed (e.g., 10 Gb/s) portions of the circuitry, C<sup>3</sup>MOS for very high speed parts of the circuit (e.g., 2.5-5 Gb/s), and conventional CMOS logic for the relatively lower speed sections. For example, to enable an integrated circuit to be used in ultra high speed applications, the input and output circuitry that interfaces with and processes the high speed signals is implemented using C<sup>3</sup>MOS with inductive broadbanding. The circuit also employs C<sup>3</sup>MOS to divide down the frequency of the signals being processed to a low enough frequency where conventional CMOS logic can be used. The core of the circuit, according to this embodiment, is therefore implemented by conventional CMOS logic that consumes zero static current.

Figure 6(b) shows an implementation of the 2:1 multiplexer 58 wherein the actual output multiplexing circuit 62 uses C<sup>3</sup>MOS with inductive broadbanding an implementation of which is shown in Figure 7.

Figure 7 shows an exemplary C<sup>3</sup>MOS with inductive broadbanding implementation for a 2:1 multiplexer 62. Similar to the other C<sup>3</sup>MOS logic gates, multiplexer 62 includes a differential pair for each input. The positive (left) input transistor of each differential pair is coupled to VDD through by a first resistor 206

connected in series with a first series inductor 208 and the negative (right) input transistor of each differential pair is coupled to VDD through by a second resistor 207 connected in series with a second series inductor 209. The multiplexer 62 further includes select transistors 502 and 504 inserted between the common  
5 source terminals of the differential pairs and the current source transistor 506. By asserting one of the select input signals SELA or SELB, the bias current is steered to the differential pair associated with that select transistor. Thus, signal SELA steers the bias current to the differential pair with AP and AN inputs, and signal SELB steers the bias current to the differential pair with BP and BN inputs.

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Figure 8 shows an exemplary implementation of a C<sup>3</sup>MOS flip flop with inductive broadbanding for use as the re-timing flip flop in the serializer of Figure 5. A C<sup>3</sup>MOS master-slave flip-flop 800 according to the present invention can be made by combining two latches 802 and 804. A first latch 802 receives  
15 differential input signals D and  $\overline{D}$  and generates differential output signals QI and  $\overline{QI}$ . The differential output signals QI and  $\overline{QI}$  are then applied to the differential inputs of a second latch 804. The differential outputs Q and  $\overline{Q}$  of second latch 804 provide the outputs of flip-flop 800. The input transistors of each latch are coupled to VDD by a resistor and shunt inductor coupled in series.

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It is to be understood that all C<sup>3</sup>MOS logic elements, numerous examples of which are described on the above-referenced commonly-assigned patent application, can employ the inductive broadbanding technique according to the present invention.

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According to one embodiment of the present invention the combined C<sup>3</sup>MOS with inductive broadbanding/C<sup>3</sup>MOS/CMOS circuit technique is employed in a transceiver of the type illustrated in Figure 9. The exemplary transceiver of Figure 9 is typically found along fiber optic channels in high speed  
30 telecommunication networks. The transceiver includes at its input a photo detect and driver circuit 1200 that receives the input signal from the fiber optic channel.

Circuit 1200 converts fiber-optic signal to packets of data and supplies it to a clock data recovery (CDR) circuit 1202. CDR circuit 1202 recovers the clock and data signals that may be in the frequency range of about 10 GHz, or higher.

Established telecommunication standards require the transceiver to perform  
5 various functions, including data monitoring and error correction. These functions are performed at a lower frequency. Thus, the transceiver uses a demultiplexer 1204, depicted in Figs. 5 and 6, which deserializes the 10 Gb/s data stream into, for example, 16 parallel signals having a bit rate of about 622 Mb/s. An application specific integrated circuit (ASIC) 1206 then performs the monitoring  
10 and error correction functions at the lower (622 Mb/s) bit rate. A multiplexer and clock multiplication unit (CMU) 1208 converts the parallel signals back into a single bit stream at 10 Gb/s. This signal is then retransmitted back onto the fiber optic channel by a laser drive 1212. The combined C<sup>3</sup>MOS with inductive  
broadbanding /C<sup>3</sup>MOS/CMOS technique of the present invention allows  
15 fabrication of demultiplexer 1204, ASIC 1206 and multiplexer and CMU 1208 on a single silicon die. That is, demultiplexer 1204 and multiplexer and CMU 1208 are implemented in C<sup>3</sup>MOS with inductive broadbanding /C<sup>3</sup>MOS with ASIC 1206 implemented in conventional CMOS.

20 In conclusion, the present invention provides various circuit techniques for implementing ultra high speed circuits using current-controlled CMOS (C<sup>3</sup>MOS) logic and C<sup>3</sup>MOS with inductive broadbanding logic fabricated in conventional CMOS process technology. In one embodiment, the present invention advantageously combines high speed C<sup>3</sup>MOS with inductive  
25 broadbanding / C<sup>3</sup>MOS with inductive broadbanding /C<sup>3</sup>MOS logic with low power conventional CMOS logic. According to this embodiment circuits such as transceivers along fiber optic channels can be fabricated on a single chip where the ultra-high speed portions of the circuit utilize C<sup>3</sup>MOS with inductive  
broadbanding /C<sup>3</sup>MOS and the relatively lower speed parts of the circuit use  
30 conventional CMOS logic.

While the above is a complete description of the preferred embodiment of the present invention, it is possible to use various alternatives, modifications and equivalents. For example, although spiral inductors and poly resistors are utilized in the preferred embodiment other techniques known to persons of skill in the art can be utilized. Therefore, the scope of the present invention should be determined not with reference to the above description but should, instead, be determined with reference to the appended claims, along with their full scope of equivalents.

WHAT IS CLAIMED IS:

- 1                   1.       A current-controlled metal-oxide-semiconductor field-effect  
2 transistor (MOSFET) circuit fabricated on a silicon substrate, comprising:  
3                   first and second n-channel MOSFETs having their source terminals  
4 coupled to a first node, their gate terminals coupled to receive a first and second  
5 differential logic signals, respectively, and their drain terminals coupled  
6 respectively to first and second output nodes;  
7                   first and second series RL circuits respectively coupled between said  
8 first and second output nodes and a logic high level;  
9                   first and second capacitive loads ( $C_L$ ) respectively coupled to said  
10 output nodes;  
11                   a current-source n-channel MOSFET coupled between the source  
12 terminals of the first and second select n-channel MOSFETs and a logic low level.
- 1                   2.       The circuit of claim 1 wherein:  
2                   the magnitude of  $C_L$ , R, and L are about equal to values determined  
3 by the relation  $L = (.35) * C_L R^2$ .
- 1                   3.       A current-controlled metal-oxide-semiconductor field-effect  
2 transistor (MOSFET) circuit fabricated on a silicon substrate, comprising:  
3                   a multiplexing circuit including:  
4                   first and second n-channel MOSFETs having their source terminals  
5 coupled to a first node, their gate terminals coupled to receive a first pair of  
6 differential logic signals, respectively, and their drain terminals coupled to a true  
7 output and a complementary output, respectively;  
8                   third and fourth n-channel MOSFETs having their source terminals  
9 coupled to a second node, their gate terminals coupled to receive a second pair of  
10 differential logic signals, and their drain terminals coupled to the true output and a  
11 complementary output, respectively;  
12                   first and second RL series circuits respectively coupling the true  
13 output and the complementary output to a logic high level;



14                   a first select n-channel MOSFET having a drain terminal coupled to  
15 the first node, a gate terminal coupled to receive a first select logic signal, and a  
16 source terminal; and

17                   a second select n-channel MOSFET having a drain terminal coupled  
18 to the second node, a gate terminal coupled to receive a second select logic signal,  
19 and a source terminal.

1                   4.       The circuit of claim 3 further comprising:

2                   first and second capacitive loads,  $C_L$ , coupled, respectively, the true  
3 and complementary outputs, with the magnitude of  $C_L$ ,  $R$ , and  $L$  are about equal to  
4 values determined by the relation  $L = (.35) * C_L R^2$ .

1                   5.       A current-controlled metal-oxide-semiconductor field-effect  
2 transistor (MOSFET) circuit fabricated on a silicon substrate, comprising a flip-  
3 flop including:

4                   a first clocked latch comprising:

5                   first and second n-channel MOSFETs having their source  
6 terminals connected together, their gate terminals coupled to receive a pair of  
7 differential logic signals, respectively, and their drain terminals connected to a first  
8 output and a second output, respectively;

9                   a first clocked n-channel MOSFET having a drain terminal  
10 coupled to the source terminals of the first and second n-channel MOSFETs, a gate  
11 terminal coupled to receive a first clock signal  $CK$ , and a source terminal;

12                   third and fourth n-channel MOSFETs having their source  
13 terminals coupled together, their gate terminals and drain terminals respectively  
14 cross-coupled to the first output and the second output;

15                   a second clocked n-channel MOSFET having a drain terminal  
16 coupled to the source terminals of the third and fourth n-channel MOSFETs, a gate  
17 terminal coupled to receive a second clock signal  $CKB$ , and a source terminal;

18                   first and second RL series circuits respectively coupling the  
19 first output and the second output to a logic high level; and

20 a second clocked latch comprising:  
21 fifth and sixth n-channel MOSFETs having their source  
22 terminals connected together, their gate terminals coupled to receive a pair of  
23 differential logic signals, respectively, and their drain terminals connected to a  
24 third output and a fourth output, respectively;  
25 a third clocked n-channel MOSFET having a drain terminal coupled  
26 to the source terminals of the fifth and sixth n-channel MOSFETs, a gate terminal  
27 coupled to receive a second clock signal CKB, and a source terminal;  
28 seventh and eighth n-channel MOSFETs having their source  
29 terminals coupled together, their gate terminals and drain terminals respectively  
30 cross-coupled to the third output and the fourth output;  
31 a fourth clocked n-channel MOSFET having a drain terminal  
32 coupled to the source terminals of the seventh and eighth n-channel MOSFETs, a  
33 gate terminal coupled to receive a first clock signal CK, and a source terminal;  
34 third and fourth LR series circuits respectively coupling the third  
35 output and the fourth output to a logic high level;  
36 wherein, the gate terminals of the fifth and sixth n-channel  
37 MOSFETs in the second clocked latch respectively couple to the first output and  
38 the second output of the first clocked latch.

1 6. The circuit of claim 3 further comprising:  
2 first and second capacitive loads,  $C_L$ , coupled, respectively, the true  
3 and complementary outputs of said second latch, with the magnitude of  $C_L$ ,  $R$ , and  
4  $L$  are about equal to values determined by the relation  $L = (.35) * C_L R^2$ .

1 7. A metal-oxide-semiconductor field-effect transistor  
2 (MOSFET) circuit fabricated on a silicon substrate, comprising:  
3 first circuitry implemented, including first and second output nodes  
4 and power supply nodes, using current-controlled complementary metal-oxide  
5 semiconductor (C3MOS) logic with inductive broadbanding wherein logic levels  
6 are signaled by current steering in one of two or more branches in response to

7 differential input signals, and wherein first and second series connected RL circuits  
8 couple, respectively, the first and second output nodes to the first and second  
9 power supply nodes, the first circuitry being configured to receive an input signal  
10 having a first frequency and to generate a first output signal having a second  
11 frequency lower than the first frequency;  
12 second circuitry implemented using current-controlled  
13 complementary metal-oxide semiconductor (C3MOS) logic wherein logic levels  
14 are signaled by current steering in one of two or more branches in response to  
15 differential input signals, the second circuitry being configured to receive said first  
16 output input signal having and to generate an second output signal having a third  
17 frequency lower than the second frequency; and  
18 third circuitry implemented using conventional complementary  
19 metal-oxide-semiconductor (CMOS) logic wherein substantially zero static current  
20 is dissipated, the second circuitry being configured to receive and process the  
21 output signal having the third frequency.

1 8. The MOSFET circuit of claim 4 wherein the first circuitry  
2 comprises an input circuit that is implemented using the C3MOS with inductive  
3 broadbanding logic, and is configured to deserialize the input signal into a plurality  
4 of lower frequency signals.

1 9. The MOSFET circuit of claim 5 wherein the second circuitry  
2 comprises conventional CMOS logic that is configured to process the plurality of  
3 lower frequency signals to generate a plurality of lower frequency processed  
4 signals.

1 10. The MOSFET circuit of claim 4 wherein the circuit comprises  
2 a transceiver, the transceiver comprising:  
3 a first input deserializer implemented by the C<sup>3</sup>MOS with inductive  
4 broadbanding logic, and configured to receive the input signal having the first  
5 frequency and to generate a plurality of parallel first signals at the second  
6 frequency;

7                   a second input deserializer implemented by the C<sup>3</sup>MOS logic, and  
8   configured to receive the first output having the second frequency and to generate  
9   a plurality of parallel third signals at the third frequency;  
10                  core circuitry implemented by the CMOS logic, and coupled to said  
11   input deserializer, the core circuitry being configured to process the plurality of  
12   parallel signal at the third frequency;  
13                  a first output serializer implemented by the C<sup>3</sup>MOS logic, and  
14   coupled to the core circuitry, the serializer being configured to receive the plurality  
15   of parallel signals and to generate a plurality of parallel second output signal at the  
16   second frequency; and  
17                  a second output serializer implemented by the C<sup>3</sup>MOS with inductive  
18   broadbanding logic, and coupled to the first serializer, the second serializer being  
19   configured to receive the plurality of parallel second signals and to generate a  
20   single output signal at the first frequency.

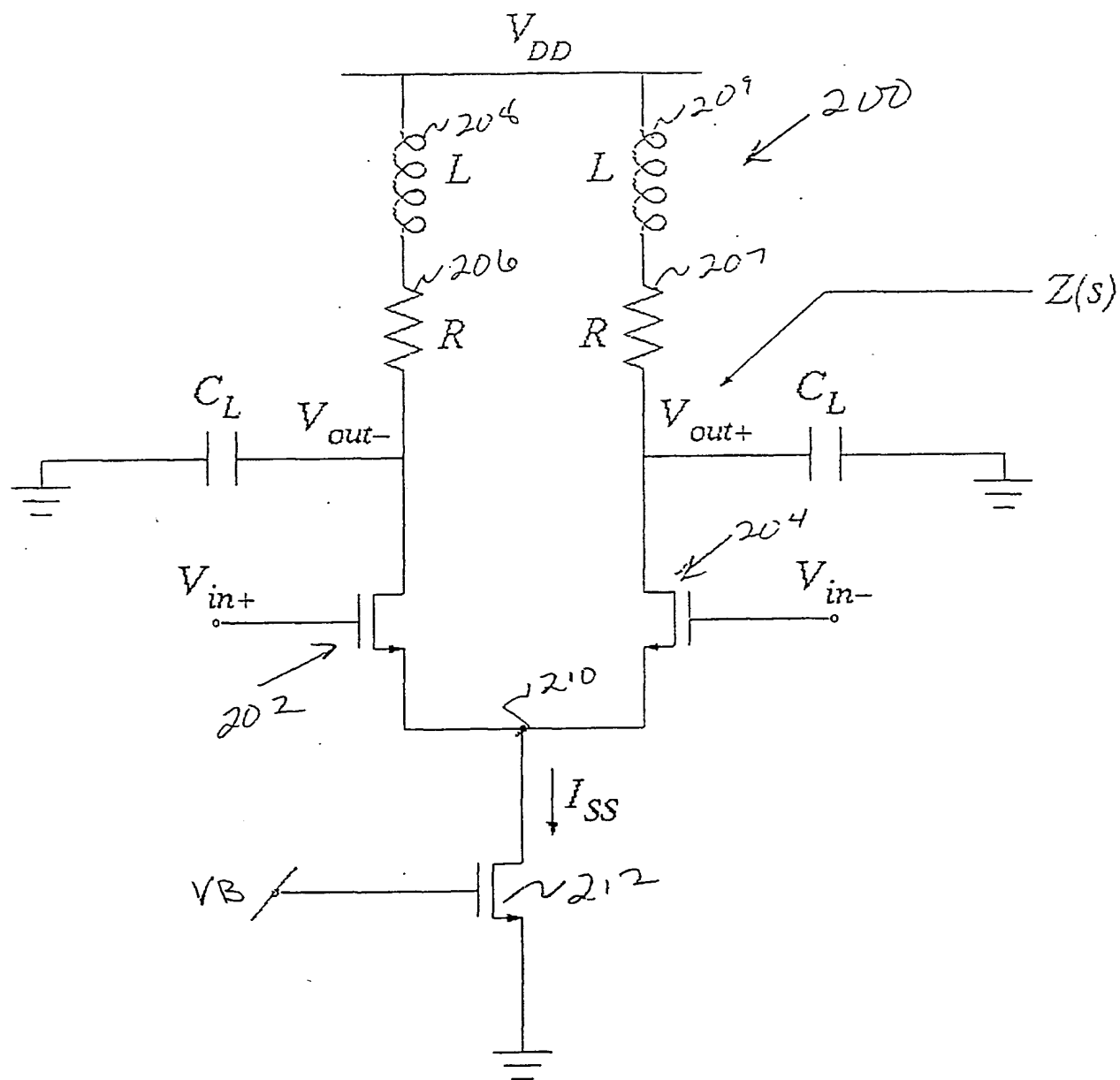


fig. 1

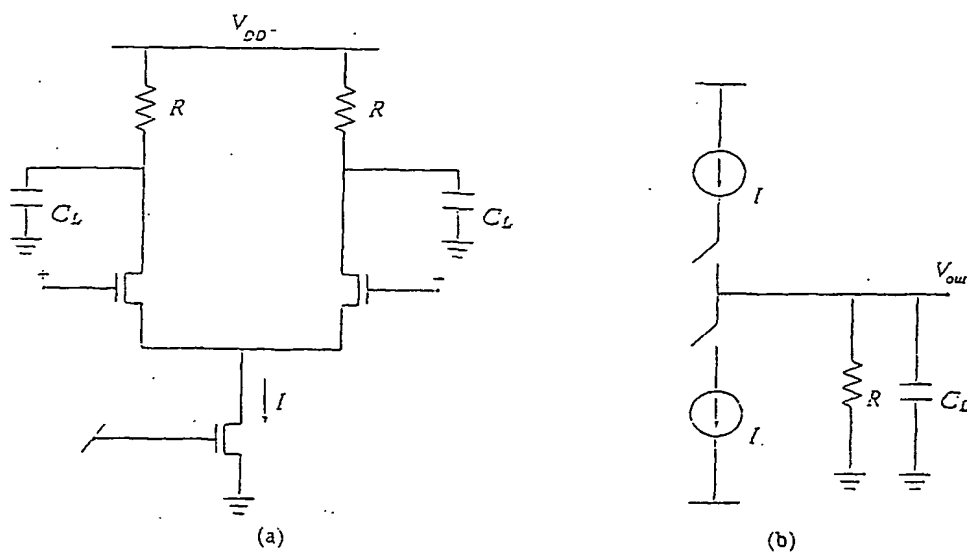


Figure 2: (a) C<sup>3</sup>MOS buffer; (b) simplified illustration of transient behavior.

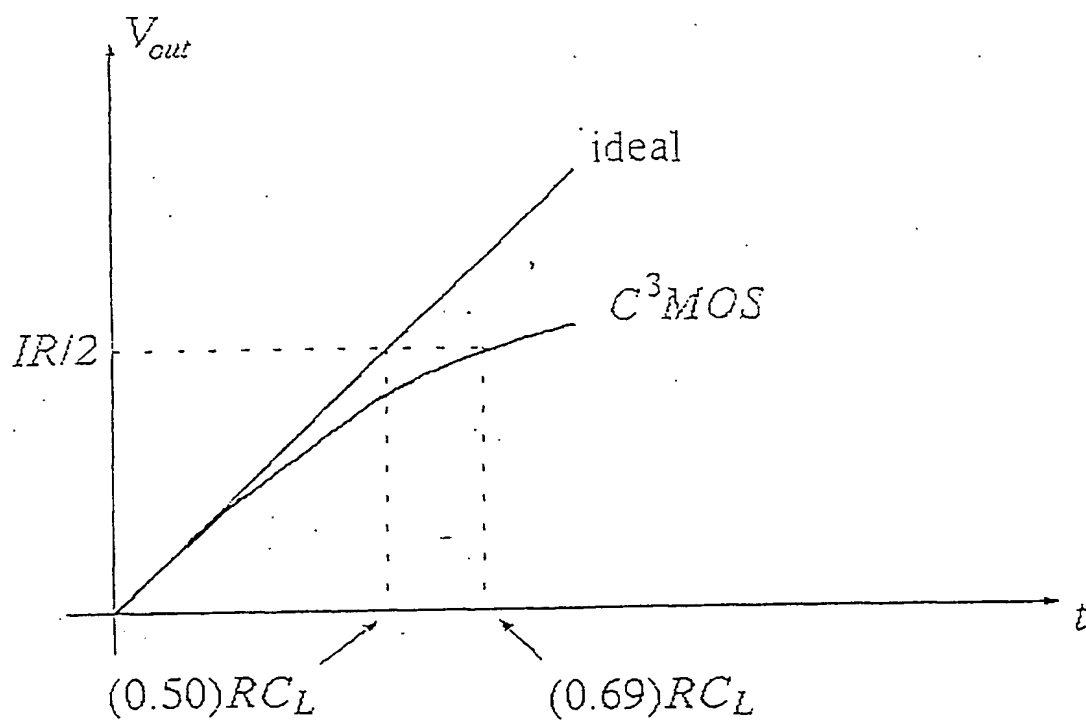


Fig. 2(c)

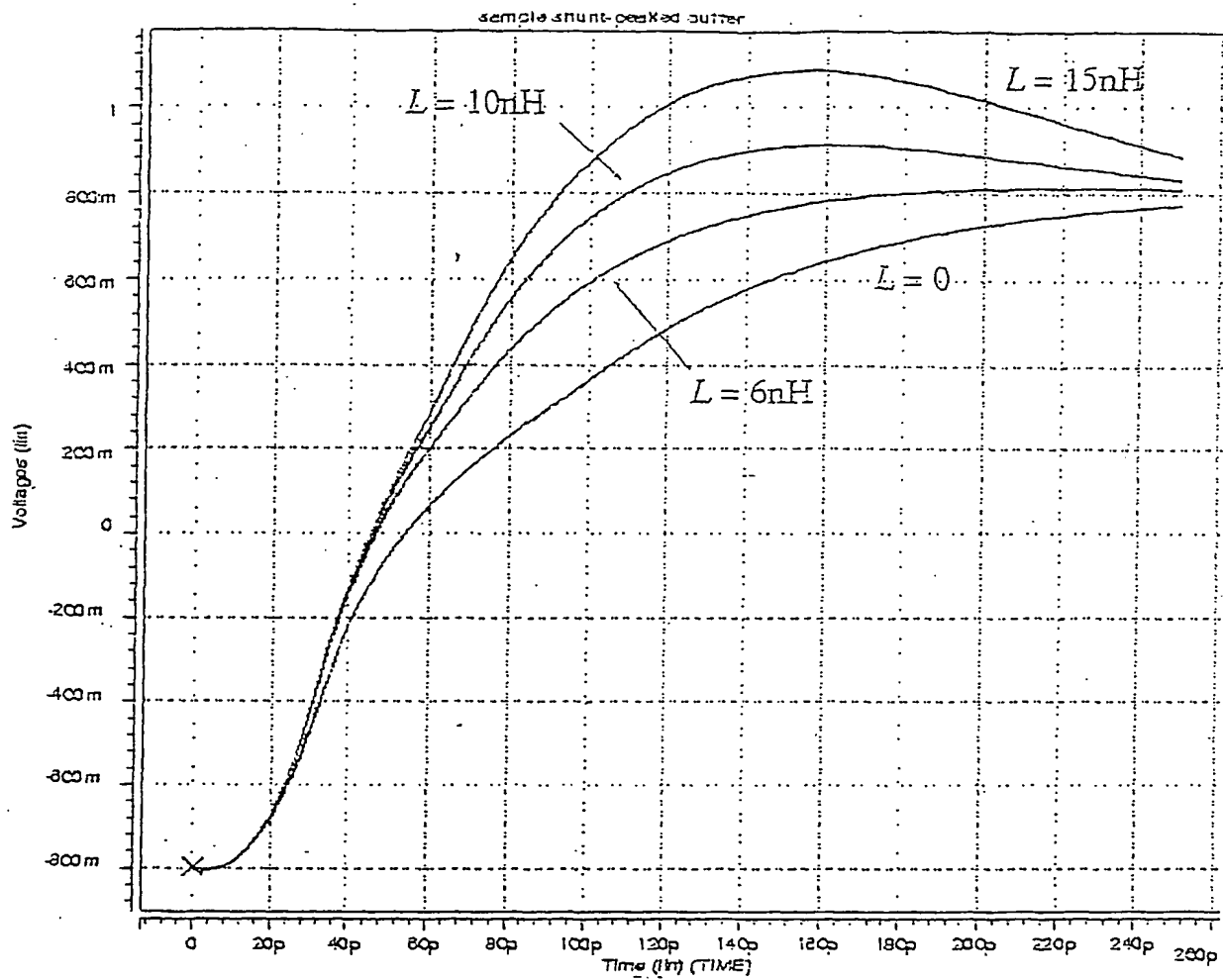
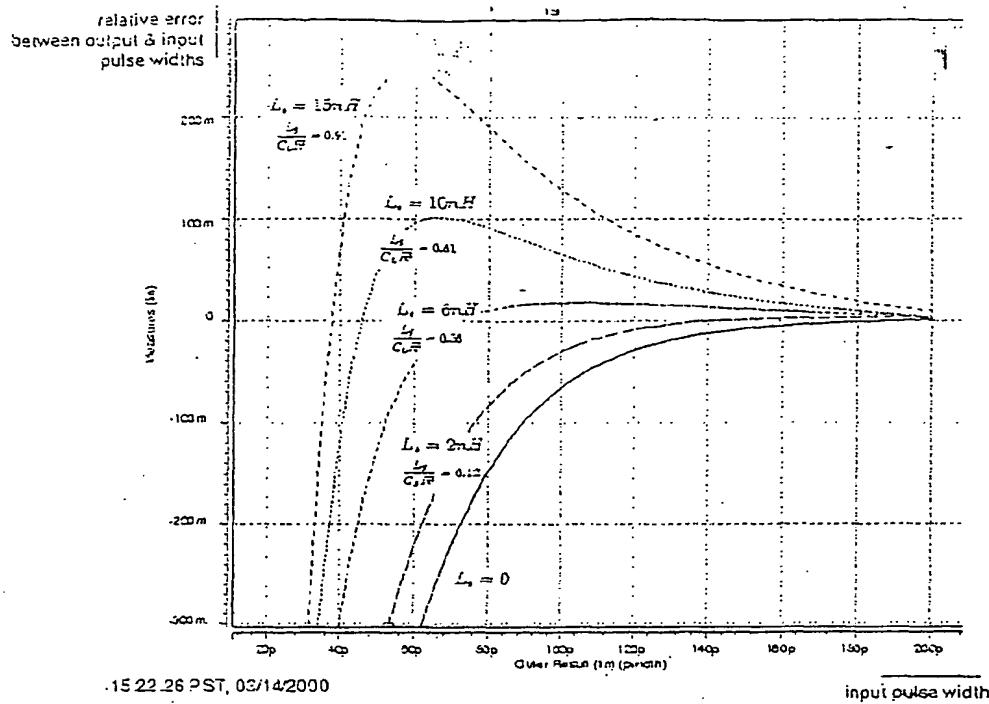


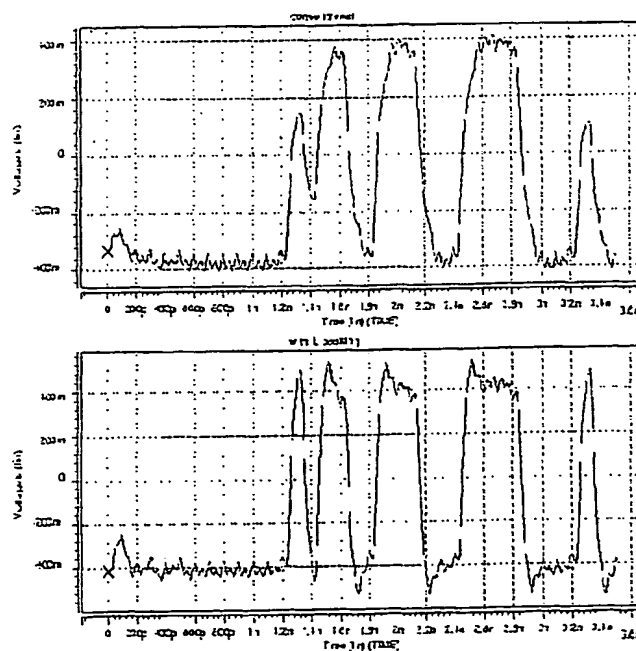
Fig. 3





Inter-symbol interference (ISI) vs. input pulse width for 5 values of series inductance.

Fig. 4(4)



conventional C3MOS blocks

C3MOS blocks with inductive peaking

Fig. 4(6)

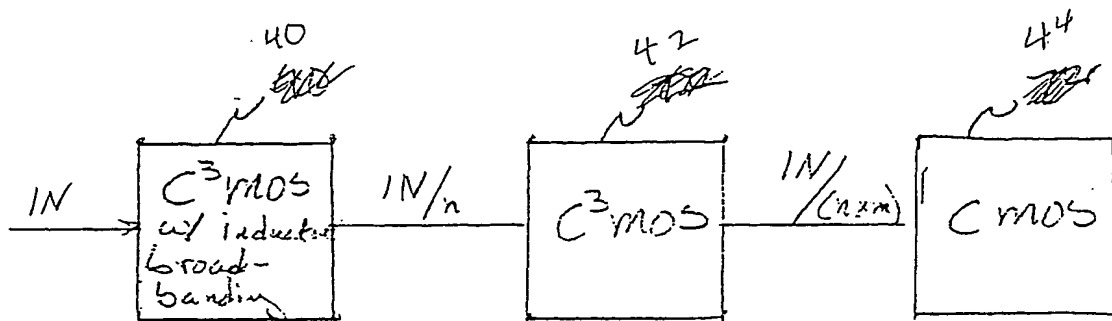
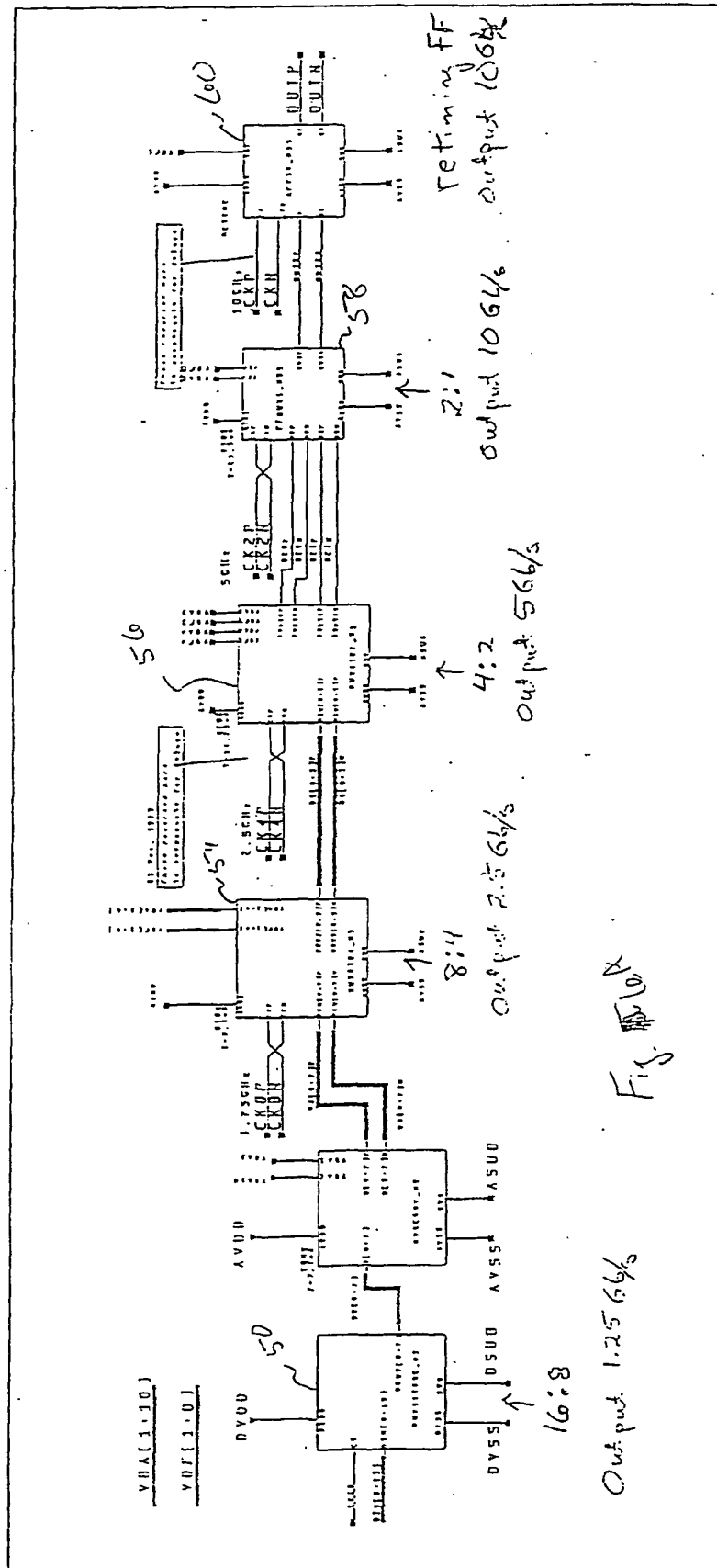


Fig. 5



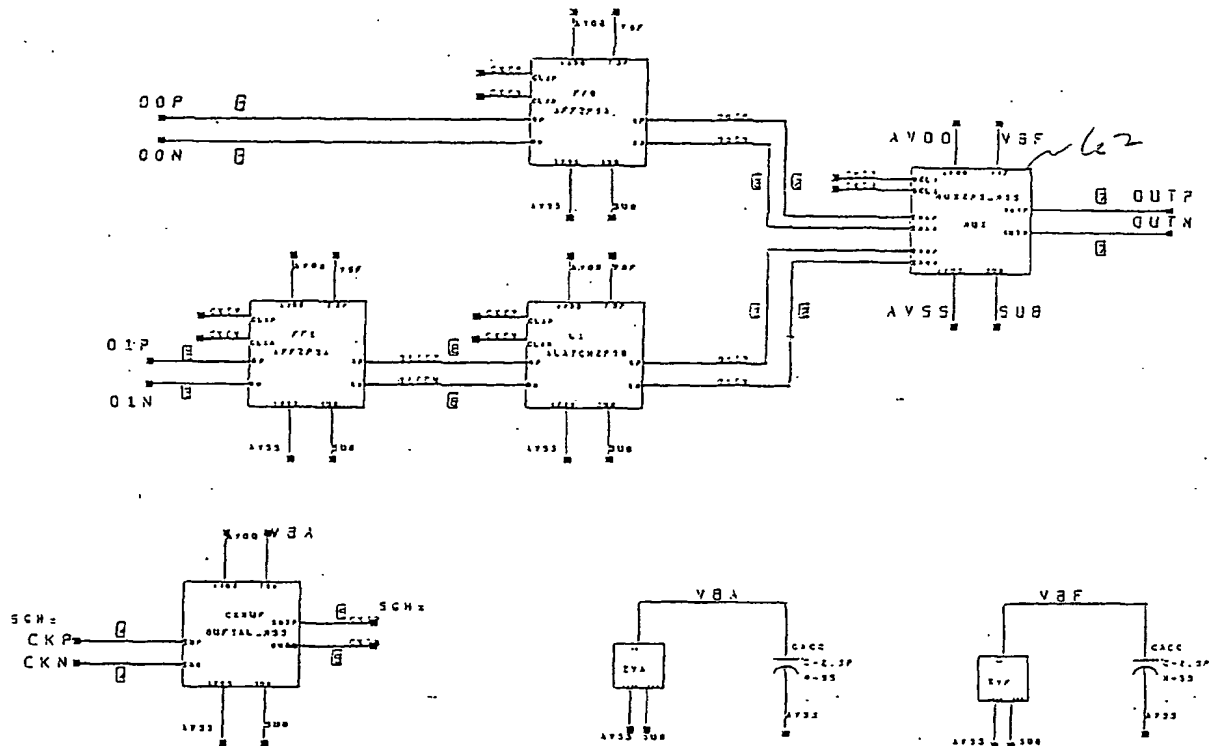
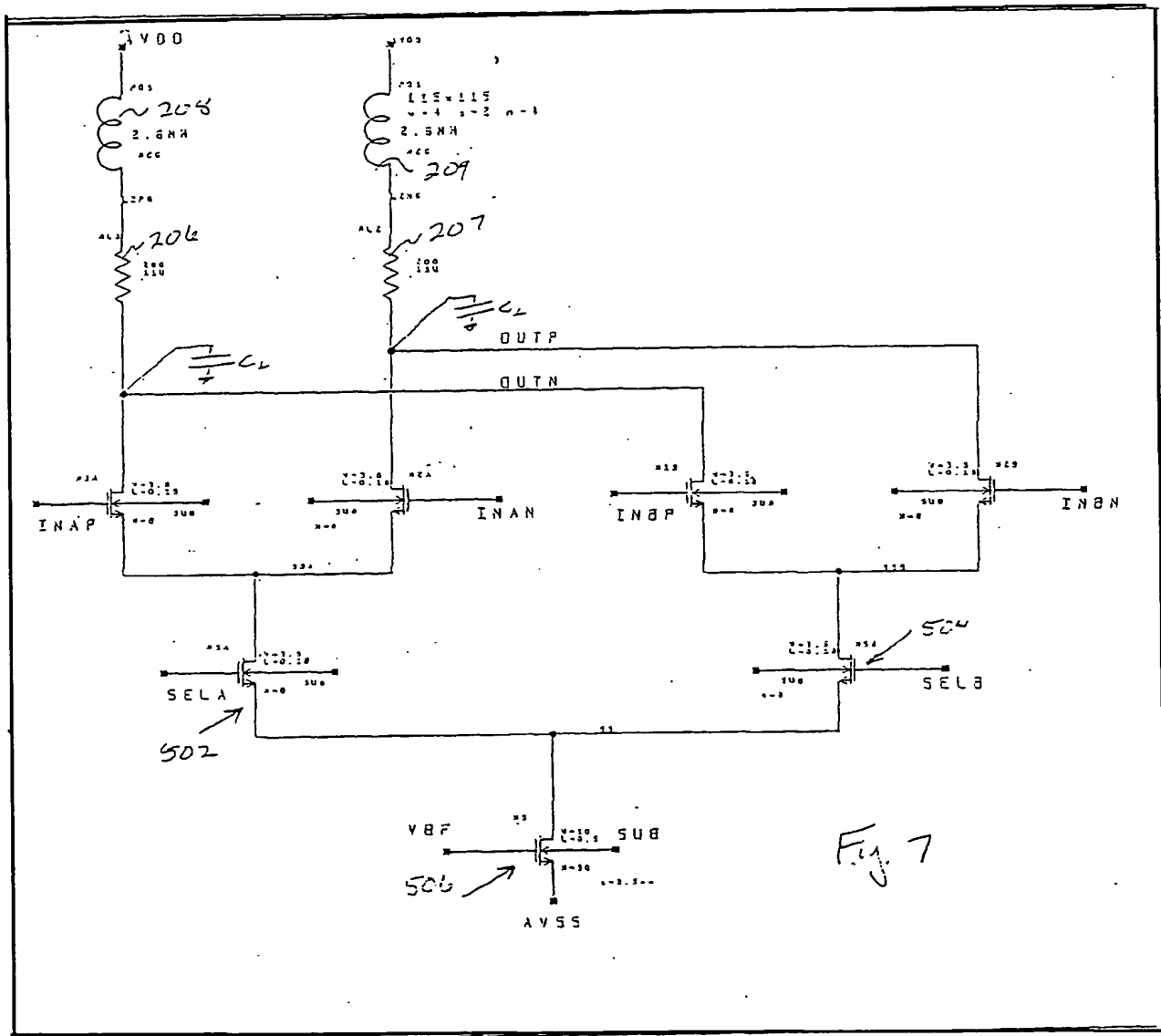
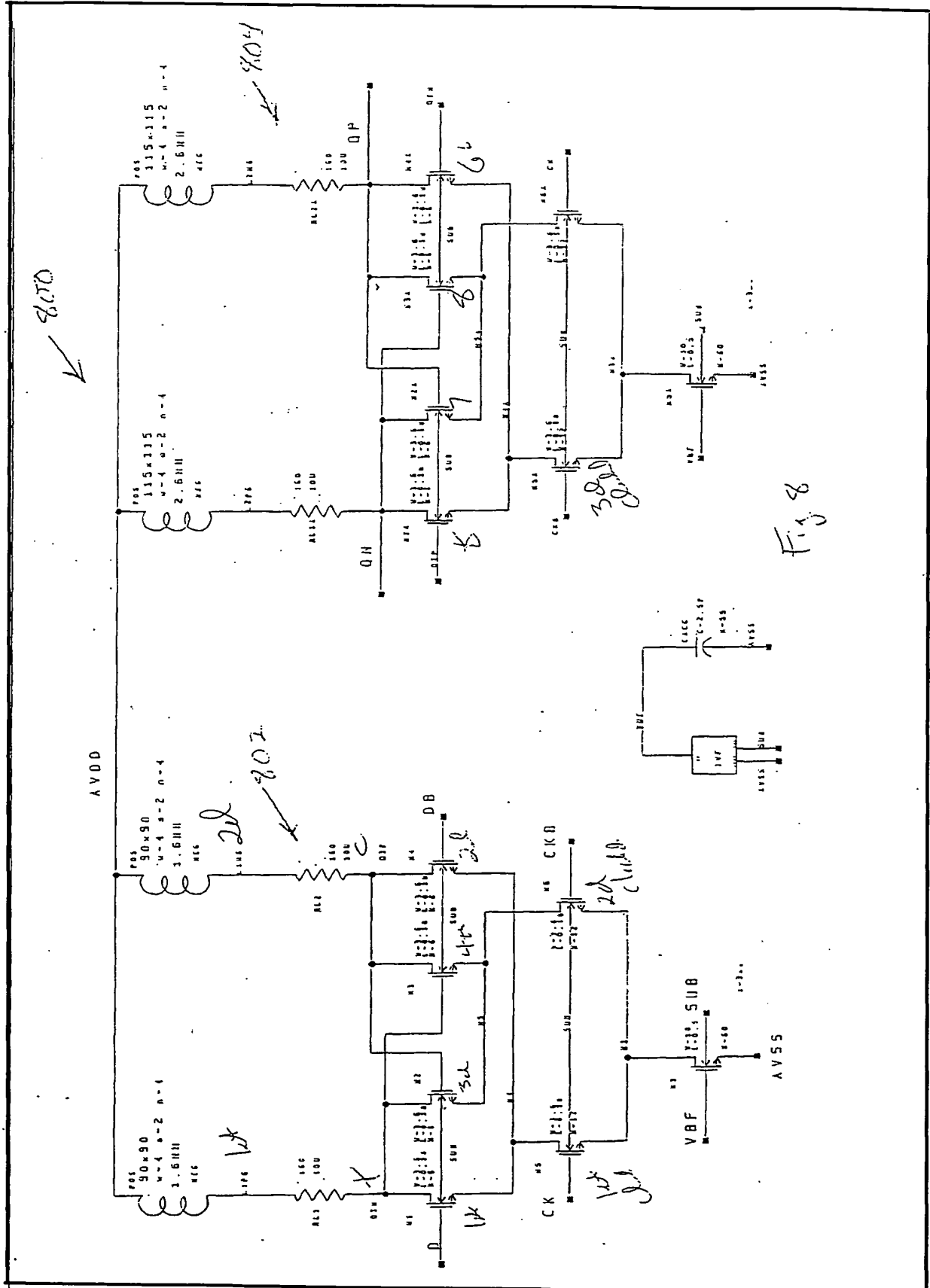
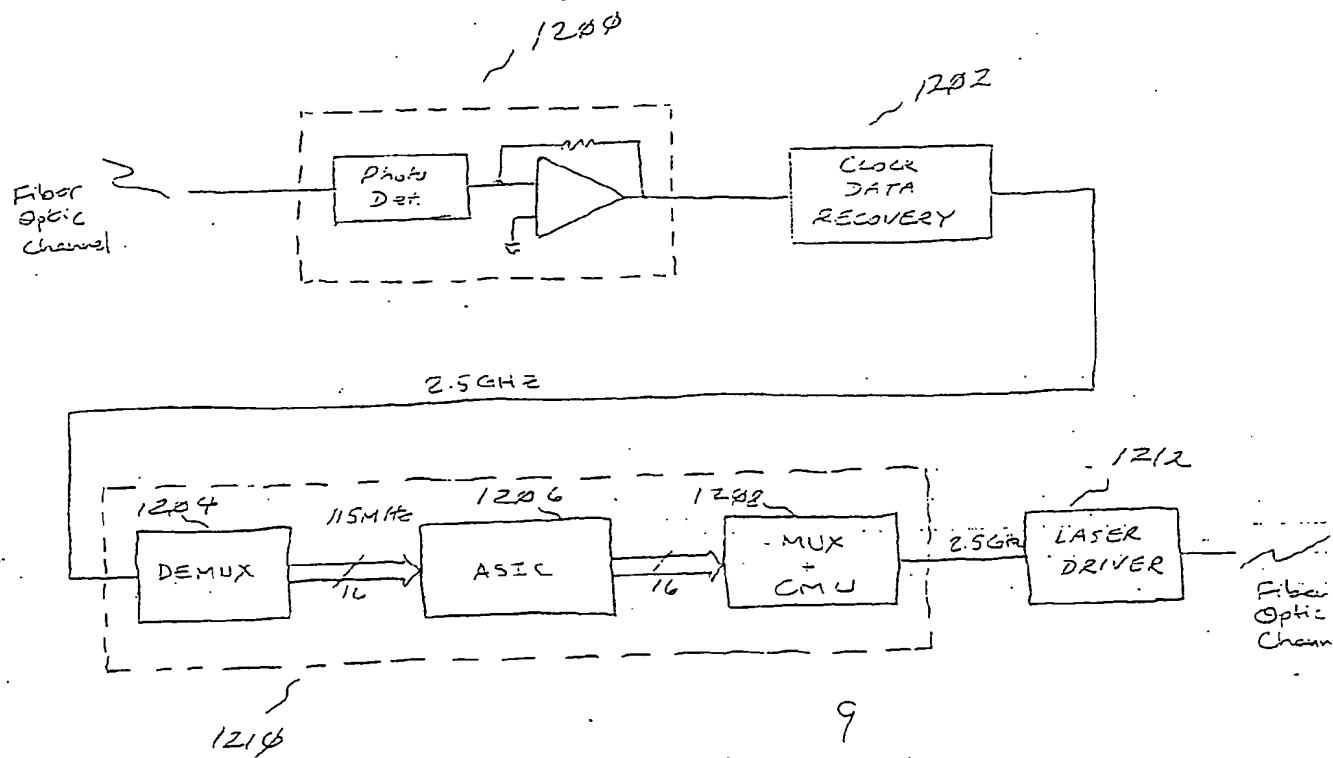


Fig. 6B







- FIGURE -

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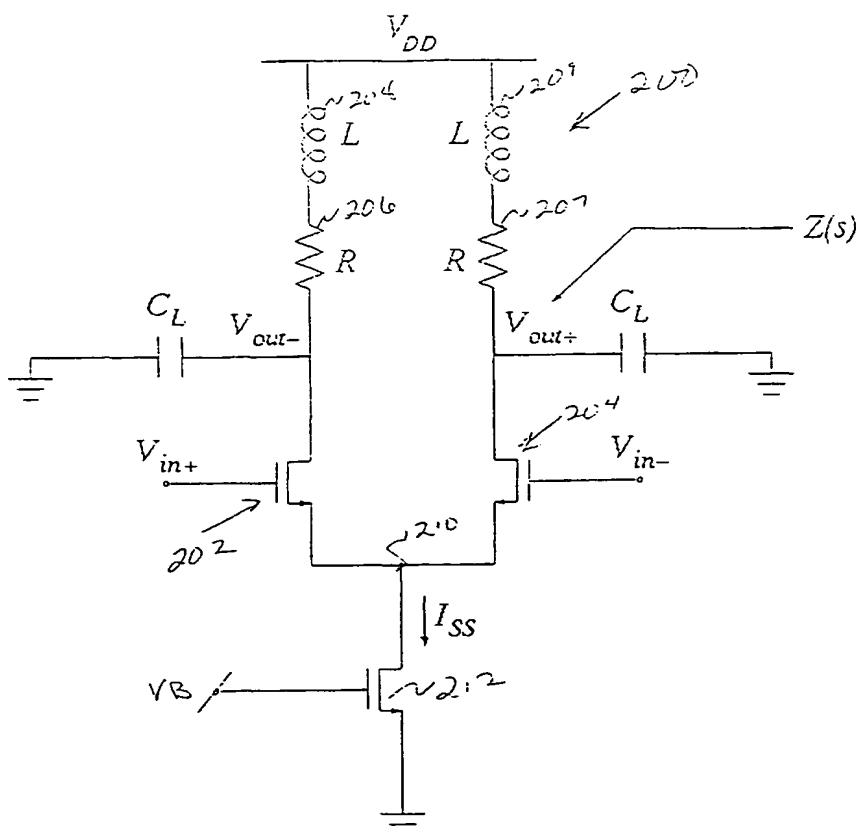
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- (72) Inventor; and  
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[Continued on next page]

(54) Title: CURRENT-CONTROLLED CMOS CIRCUITS WITH INDUCTIVE BROADBANDING



(57) Abstract: Various circuit techniques for implementing ultra high speed circuits use current-controlled CMOS (C<sup>3</sup>MOS) logic with inductive broadbanding fabricated in conventional CMOS process technology. Optimum balance between power consumption and speed for each circuit application is achieved by combining high speed C<sup>3</sup>MOS logic with inductive broadbanding /C<sup>3</sup>MOS logic with low power conventional CMOS logic. The combined C<sup>3</sup>MOS logic with inductive broadbanding /C<sup>3</sup>MOS /CMOS logic allows greater integration of circuits such as high speed transceivers used in fiber optic communication systems.

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# INTERNATIONAL SEARCH REPORT

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IPC 7 H03K19/017 H03K19/094 H03K17/0416 H03K17/693

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## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)  
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	RUDELL J C ET AL: "A 1.9-GHZ WIDE-BAND IF DOUBLE CONVERSION CMOS RECEIVER FOR CORDLESSTELEPHONE APPLICATIONS" IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE INC. NEW YORK, US, vol. 32, no. 12, 1 December 1997 (1997-12-01), pages 2071-2088, XP000767456 ISSN: 0018-9200 page 2077, right-hand column, line 33 -page 2078, left-hand column, line 9; figure 10	1
A	US 4 806 796 A (BUSHEY THOMAS P ET AL) 21 February 1989 (1989-02-21) column 3, line 57 - line 66; figure 5 column 4, line 48 -column 5, line 10; figures 8,10	1

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International Application No  
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Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Information on patent family members

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			DE 69514417 T2	24-08-2000
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